

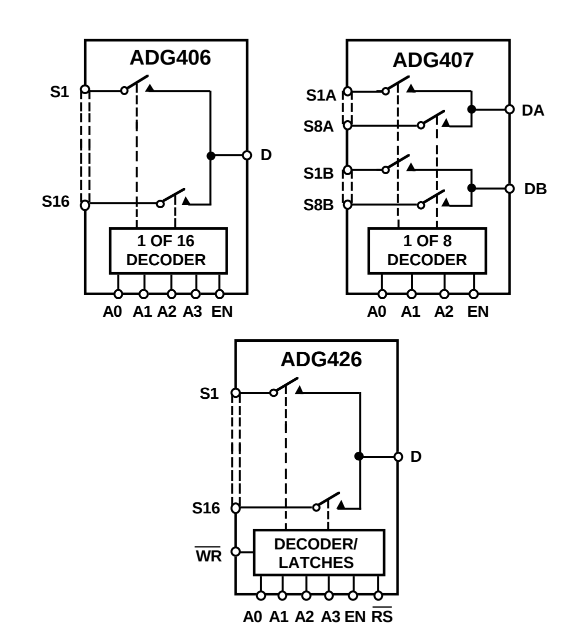
LC²MOS 8-/16-Channel High Performance Analog Multiplexers

ADG406/ADG407/ADG426

FEATURES
44 V Supply Maximum Ratings
V_{SS} to V_{DD} Analog Signal Range
Low On Resistance (80 Ω max)
Low Power
Fast Switching
t_{ON} < 160 ns
t_{OFF} < 150 ns
Break Before Make Switching Action
Plug-In Upgrade for
DG506A/ADG506A, DG507A/ADG507A, DG526/ADG526A
ADG406/ADG407 are Plug-In Replacements for DG406/DG407

APPLICATIONS
Audio and Video Routing
Automatic Test Equipment
Data Acquisition Systems
Battery Powered Systems
Sample Hold Systems
Communication Systems
Avionics

FUNCTIONAL BLOCK DIAGRAMS



GENERAL DESCRIPTION

The ADG406, ADG407 and ADG426 are monolithic CMOS analog multiplexers. The ADG406 and ADG426 switch one of sixteen inputs to a common output as determined by the 4-bit binary address lines A0, A1, A2 and A3. The ADG426 has on-chip address and control latches that facilitate microprocessor interfacing. The ADG407 switches one of eight differential inputs to a common differential output as determined by the 3-bit binary address lines A0, A1 and A2. An EN input on all devices is used to enable or disable the device. When disabled, all channels are switched OFF.

The ADG406/ADG407/ADG426 are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance. These features make the parts suitable for high speed data acquisition systems and audio signal switching. Low power dissipation makes the parts suitable for battery powered systems. Each channel conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break before make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
   The ADG406/ADG407/ADG426 are fabricated on an enhanced LC²MOS process giving an increased signal range which extends to the supply rails
2. Low Power Dissipation
3. Low R_{ON}
4. Single/Dual Supply Operation
5. Single Supply Operation
   For applications where the analog signal is unipolar, the ADG406/ADG407/ADG426 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply and will remain functional with single supplies as low as +5 V.

REV. 0

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ADG406/ADG407/ADG426–SPECIFICATIONS[1]

DUAL SUPPLY (V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	50		50		Ω typ	V_D = ±10 V, I_S = –1 mA
	80	125	80	125	Ω max	V_{DD} = +13.5 V, V_{SS} = –13.5 V
R_{ON} Match	4		4		Ω typ	V_D = 0 V, I_S = –1 mA
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
Source OFF Leakage I_S (OFF)	±0.5	±20	±0.5	±50	nA max	V_D = ±10 V, V_S = ∓10 V, Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = ±10 V, V_S = ∓10 V;
ADG406, ADG426	±1	±20	±1	±200	nA max	Test Circuit 3
ADG407	±1	±20	±1	±100	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = ±10 V;
ADG406, ADG426	±1	±20	±1	±200	nA max	Test Circuit 4
ADG407	±1	±20	±1	±100	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	μA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	120		120		ns typ	R_L = 300 Ω, C_L = 35 pF;
	150	250	150	250	ns max	V_1 = ±10 V, V_2 = ∓10 V;
						Test Circuit 5
Break Before Make Delay, t_{OPEN}	10	10	10	10	ns min	R_L = 300 Ω, C_L = 35 pF;
						V_S = +5 V, Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	120	175	120	175	ns typ	R_L = 300 Ω, C_L = 35 pF;
	160	225	160	225	ns max	V_S = +5 V, Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	110	130	110	130	ns typ	R_L = 300 Ω, C_L = 35 pF;
	150	180	150	180	ns max	V_S = +5 V, Test Circuit 7
ADG426 Only						
t_W, Write Pulse Width		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	V_S = +5 V
Charge Injection	8		8		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF;
						Test Circuit 10
OFF Isolation	–75		–75		dB typ	R_L = 1 kΩ, f = 100 kHz;
						V_{EN} = 0 V, Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, f = 100 kHz, Test Circuit 12
C_S (OFF)	5		5		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG406, ADG426	50		50		pF typ	
ADG407	25		25		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG406, ADG426	60		60		pF typ	
ADG407	40		40		pF typ	
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = –16.5 V
I_{DD}		1		1	μA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5		5	μA max	
I_{SS}		1		1	μA typ	
		5		5	μA max	
I_{DD}	100		100		μA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	200	500	μA max	
I_{SS}		1		1	μA typ	
		5		5	μA max	

NOTES

[1] Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.

[2] Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY (V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted)

Parameter	B Version +25°C	B Version –40°C to +85°C	T Version +25°C	T Version –55°C to +125°C	Units	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	90		90		Ω typ	V_D = +3 V, +8.5 V, I_S = –1 mA;
	125	200	125	200	Ω max	V_{DD} = +10.8 V
LEAKAGE CURRENTS						V_{DD} = +13.2 V
Source OFF Leakage I_S (OFF)	±0.5	±20	±0.5	±50	nA max	V_D = 8 V/0.1 V, V_S = 0.1 V/8 V; Test Circuit 2
Drain OFF Leakage I_D (OFF)						V_D = 8 V/0.1 V, V_S = 0.1 V/8 V;
ADG406, ADG426	±1	±20	±1	±200	nA max	Test Circuit 3
ADG407	±1	±20	±1	±100	nA max	
Channel ON Leakage I_D, I_S (ON)						V_S = V_D = 8 V/0.1 V, Test Circuit 4
ADG406, ADG426	±1	±20	±1	±200	nA max	
ADG407	±1	±20	±1	±100	nA max	
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current						
I_{INL} or I_{INH}		±1		±1	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]						
$t_{TRANSITION}$	180		180		ns typ	R_L = 300 Ω, C_L = 35 pF;
	220	350	220	350	ns max	V_1 = 8 V/0 V, V_2 = 0 V/8 V; Test Circuit 5
Break Before Make Delay, t_{OPEN}	10		10		ns typ	R_L = 300 Ω, C_L = 35 pF; V_S = +5 V, Test Circuit 6
t_{ON} (EN, $\overline{WR}$)	180		180		ns typ	R_L = 300 Ω, C_L = 35 pF;
	240	350	240	350	ns max	V_S = +5 V, Test Circuit 7
t_{OFF} (EN, $\overline{RS}$)	135		135		ns typ	R_L = 300 Ω, C_L = 35 pF;
	180	220	180	220	ns max	V_S = +5 V, Test Circuit 7
ADG426 Only						
t_W, Write Pulse Width		100		100	ns min	
t_S, Address, Enable Setup Time		100		100	ns min	
t_H, Address, Enable Hold Time		10		10	ns min	
t_{RS}, Reset Pulse Width		100		100	ns min	V_S = +5 V
Charge Injection	5		5		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; Test Circuit 10
OFF Isolation	–75		–75		dB typ	R_L = 1 kΩ, f = 100 kHz; Test Circuit 11
Channel-to-Channel Crosstalk	85		85		dB typ	R_L = 1 kΩ, f = 100 kHz; Test Circuit 12
C_S (OFF)	8		8		pF typ	f = 1 MHz
C_D (OFF)						f = 1 MHz
ADG406, ADG426	80		80		pF typ	
ADG407	40		40		pF typ	
C_D, C_S (ON)						f = 1 MHz
ADG406, ADG426	100		100		pF typ	
ADG407	50		50		pF typ	
POWER REQUIREMENTS						V_{DD} = +13.2 V
I_{DD}		1		1	µA typ	V_{IN} = 0 V, V_{EN} = 0 V
		5		5	µA max	
I_{DD}	100		100		µA typ	V_{IN} = 0 V, V_{EN} = 2.4 V
	200	500	200	500	µA max	

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C; T Versions: –55°C to +125°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

V_{DD} to V_{SS} . . . . +44 V
V_{DD} to GND . . . . –0.3 V to +25 V
V_{SS} to GND . . . . +0.3 V to –25 V
Analog, Digital Inputs[2]. . . . . V_{SS} – 2 V to V_{DD} + 2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D . . . . 20 mA
Peak Current, S or D . . . . 40 mA (Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range
  Industrial (B Version) . . . . –40°C to +85°C
  Extended (T Version) . . . . –55°C to +125°C
Storage Temperature Range . . . . –65°C to +150°C
Junction Temperature . . . . +150°C
Plastic Package
  θ_{JA}, Thermal Impedance . . . . 75°C/W
  Lead Temperature, Soldering (10 sec) . . . . +260°C
PLCC Package
  θ_{JA}, Thermal Impedance . . . . 80°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C
SSOP Package
  θ_{JA}, Thermal Impedance . . . . 122°C/W
  Lead Temperature, Soldering
    Vapor Phase (60 sec) . . . . +215°C
    Infrared (15 sec) . . . . +220°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]Overvoltages at A, S, D, $\overline{WR}$ or $\overline{RS}$ will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG406BN	–40°C to +85°C	N-28
ADG406BP	–40°C to +85°C	P-28A
ADG407BN	–40°C to +85°C	N-28
ADG407BP	–40°C to +85°C	P-28A
ADG426BN	–40°C to +85°C	N-28
ADG426BRS	–40°C to +85°C	RS-28

*N = Plastic DIP, P = Plastic Leaded Chip Carrier (PLCC), RS = Shrink Small Outline Package (SSOP).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



Table I. Truth Table (ADG406)

A3	A2	A1	A0	EN	ON SWITCH
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

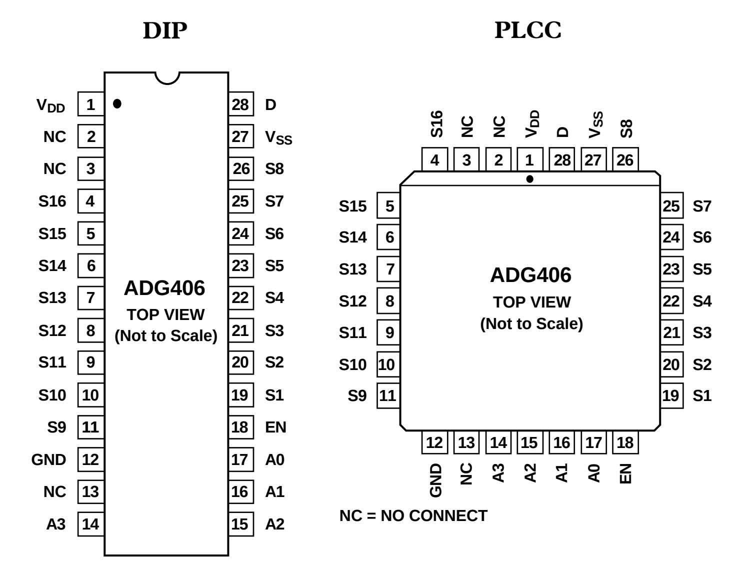
Table II. Truth Table (ADG407)

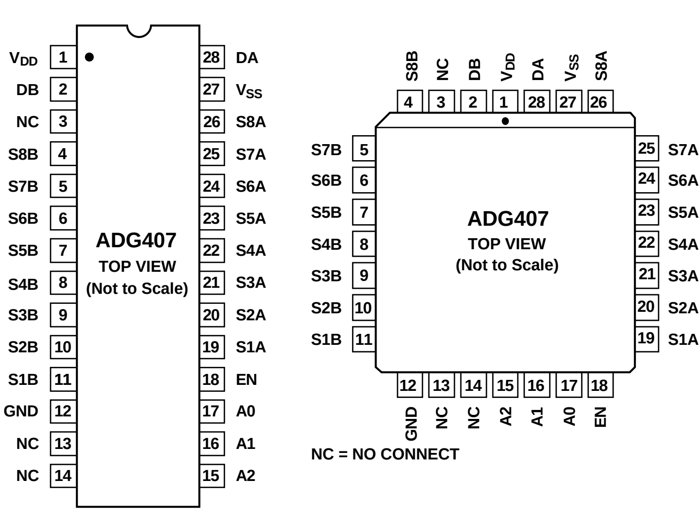
A2	A1	A0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Table III. Truth Table (ADG426)

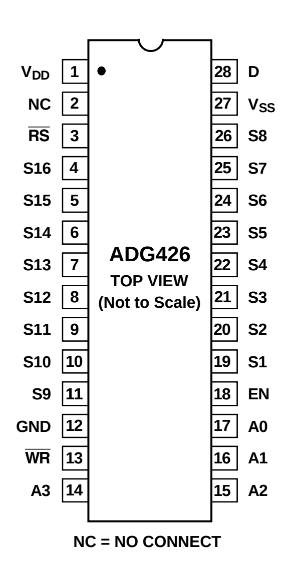
A3	A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	X	↑	1	Retains Previous Switch Condition
X	X	X	X	X	X	0	NONE (Address and Enable Latches Cleared)
X	X	X	X	0	0	1	NONE
0	0	0	0	1	0	1	1
0	0	0	1	1	0	1	2
0	0	1	0	1	0	1	3
0	0	1	1	1	0	1	4
0	1	0	0	1	0	1	5
0	1	0	1	1	0	1	6
0	1	1	0	1	0	1	7
0	1	1	1	1	0	1	8
1	0	0	0	1	0	1	9
1	0	0	1	1	0	1	10
1	0	1	0	1	0	1	11
1	0	1	1	1	0	1	12
1	1	0	0	1	0	1	13
1	1	0	1	1	0	1	14
1	1	1	0	1	0	1	15
1	1	1	1	1	0	1	16

PIN CONFIGURATIONS





PIN CONFIGURATION DIP/SSOP



TIMING DIAGRAMS (ADG426)

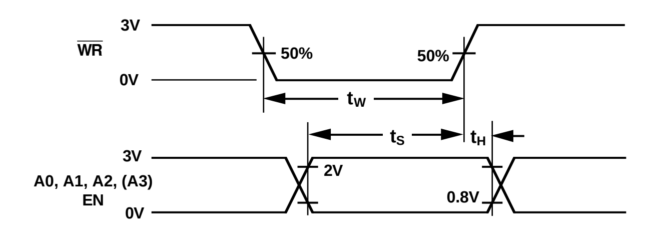


Figure 1.

Figure 1 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while $\overline{WR}$ is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of $\overline{WR}$.

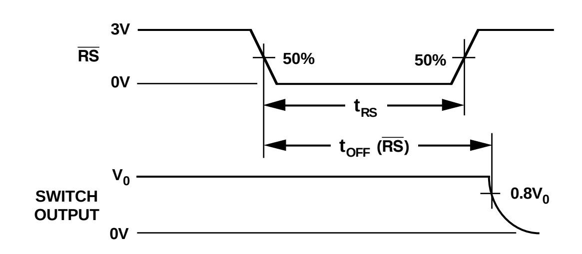


Figure 2.

Figure 2 shows the Reset Pulse Width, t_{RS}, and the Reset Turn Off Time, t_{OFF} ($\overline{RS}$).

Note: All digital input signals rise and fall times are measured from 10% to 90% of 3 V. $t_R = t_F = 20$ ns.

TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
R_{ON} Match	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for "OFF" condition.
C_D (OFF)	Channel output capacitance for "OFF" condition.
C_D, C_S (ON)	"ON" switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
t_{OPEN}	"OFF" time measured between 80% points of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for logic "0."
V_{INH}	Minimum input voltage for logic "1."
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

Typical Performance Graphs

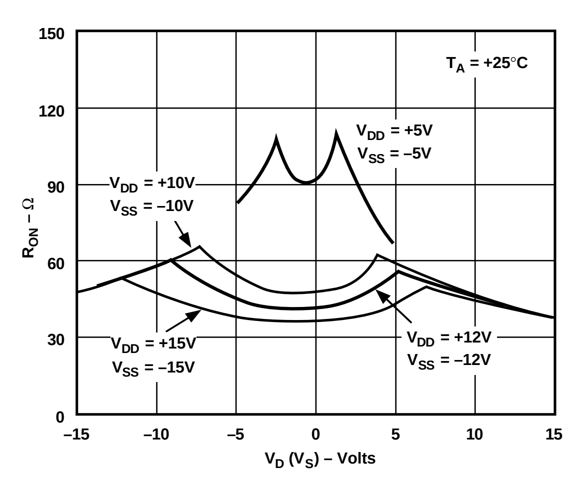


Figure 3. R_{ON} as a Function of V_D (V_S): Dual Supplies

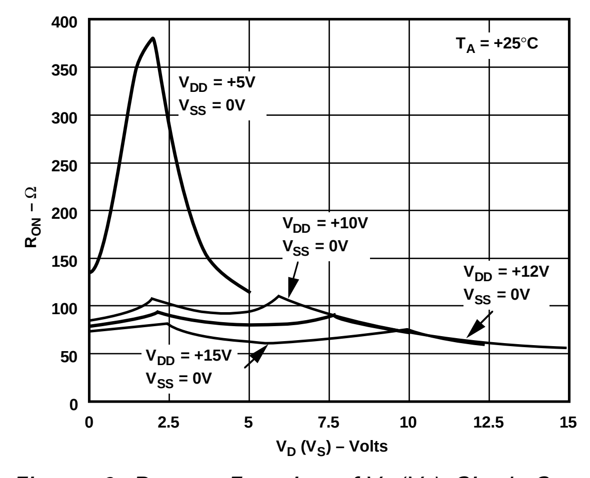


Figure 6. R_{ON} as a Function of V_D (V_S): Single Supplies

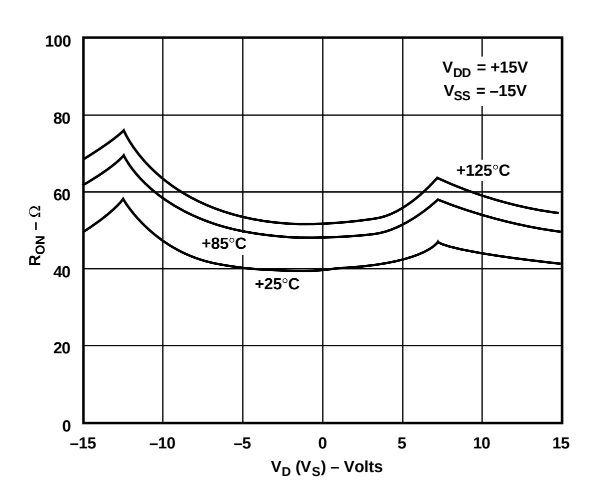


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

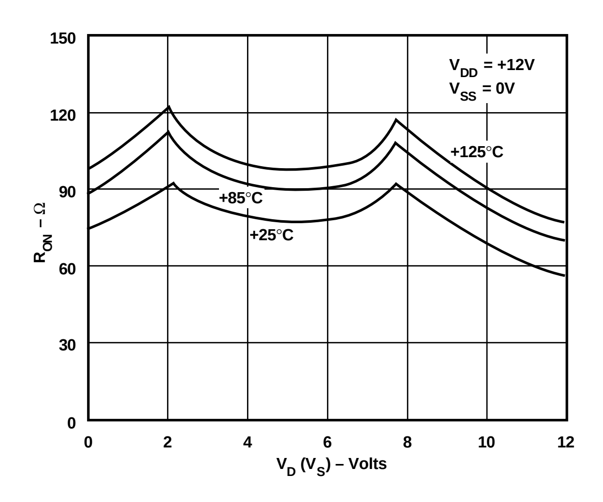


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures

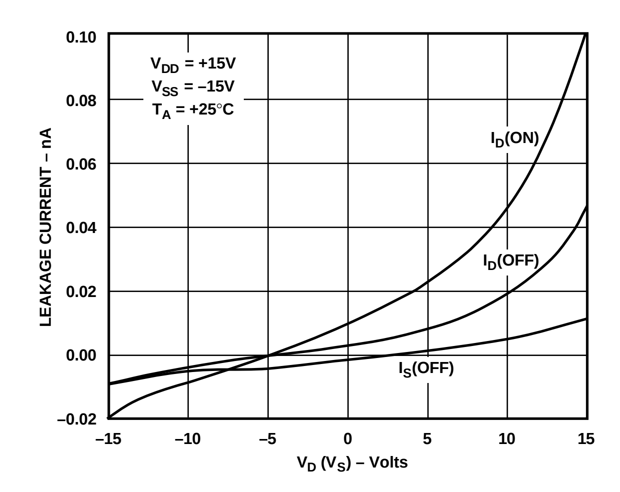


Figure 5. Leakage Currents as a Function of V_D (V_S)

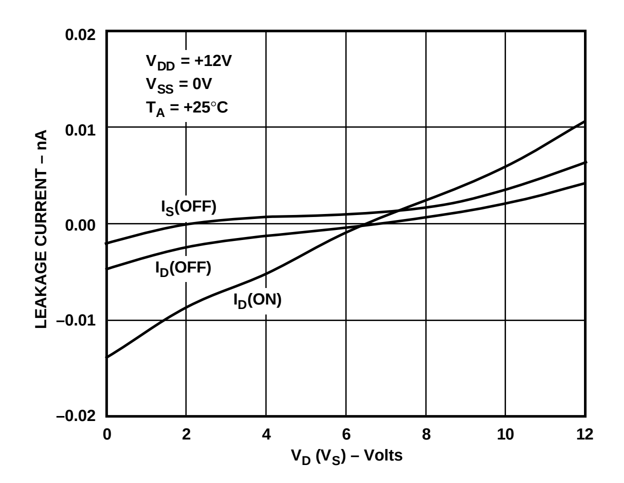


Figure 8. Leakage Currents as a Function of V_D (V_S)

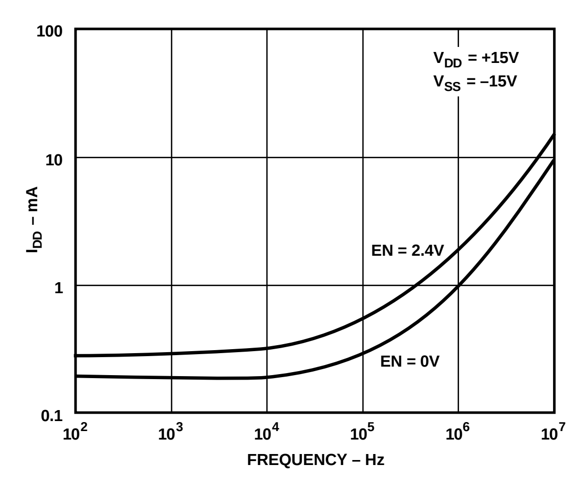


Figure 9. Positive Supply Current vs. Switching Frequency

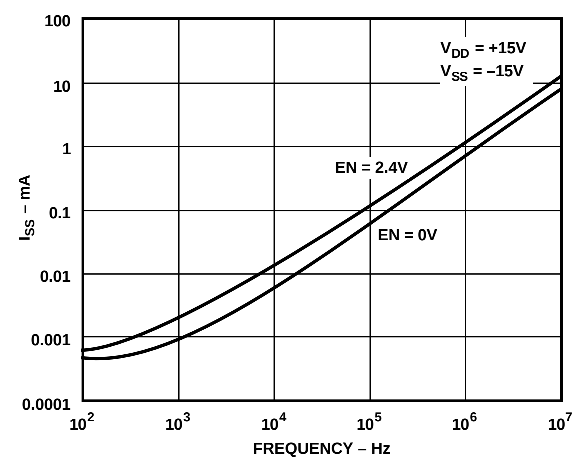


Figure 12. Negative Supply Current vs. Switching Frequency

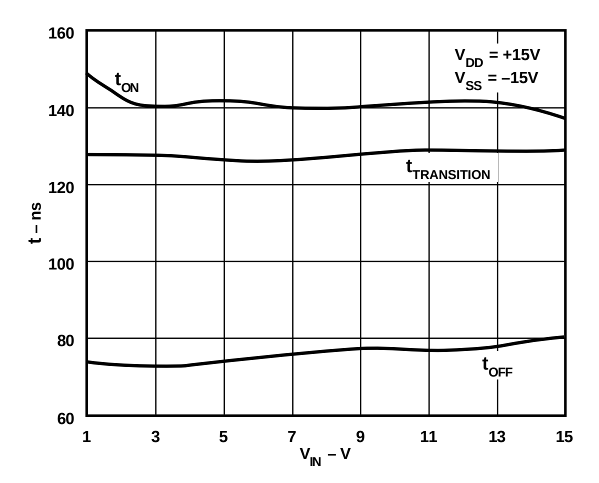


Figure 10. Switching Time vs. V_{IN} (Bipolar Supply)

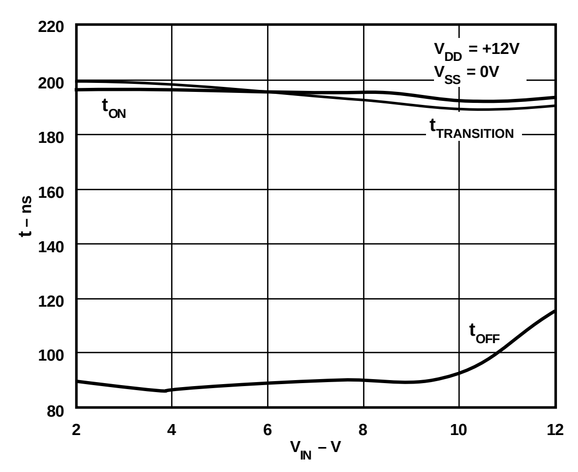


Figure 13. Switching Time vs. V_{IN} (Single Supply)

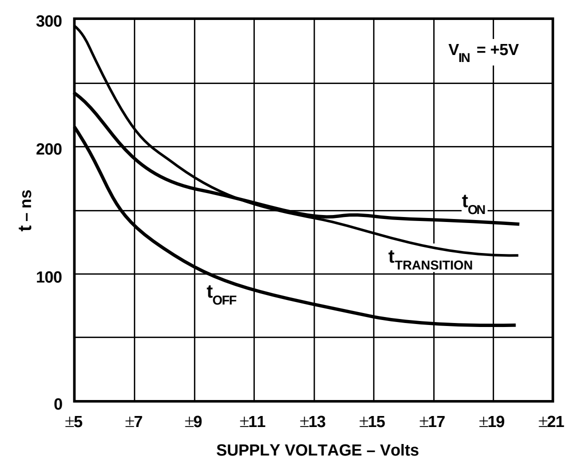


Figure 11. Switching Time vs. Bipolar Supply

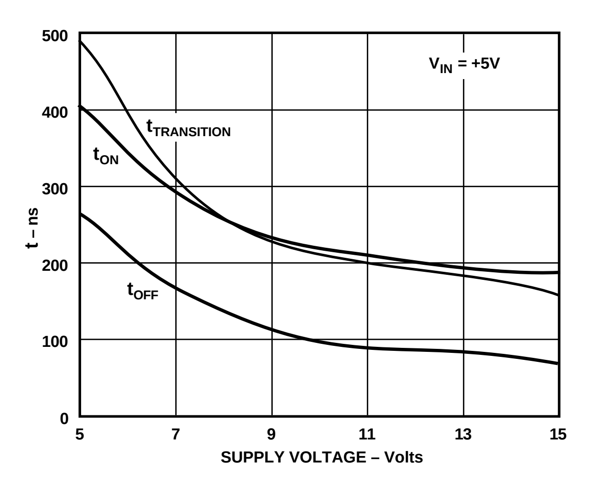


Figure 14. Switching Time vs. Single Supply

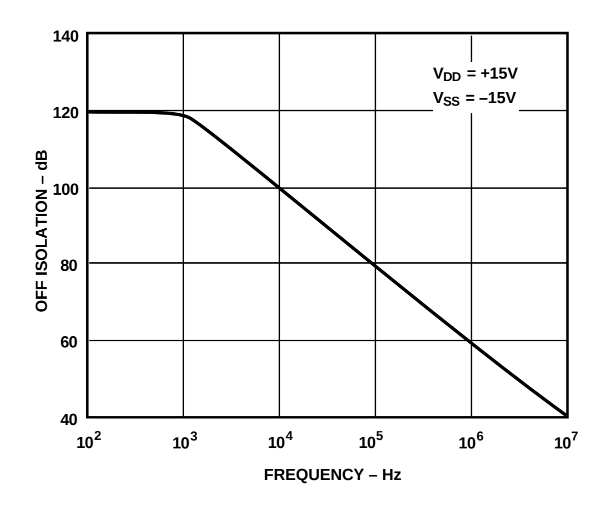


Figure 15. OFF Isolation vs. Frequency

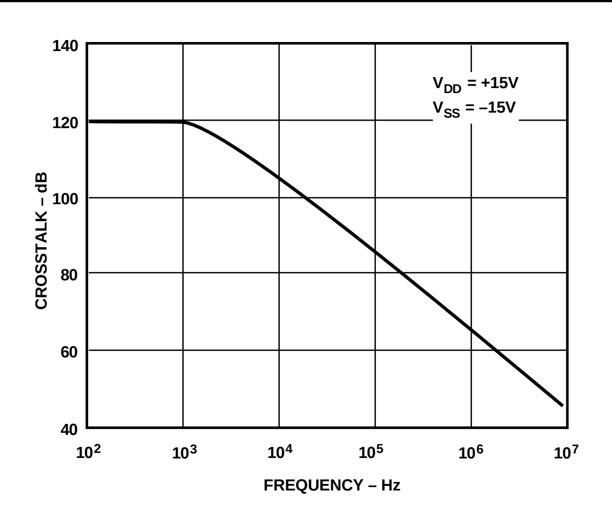
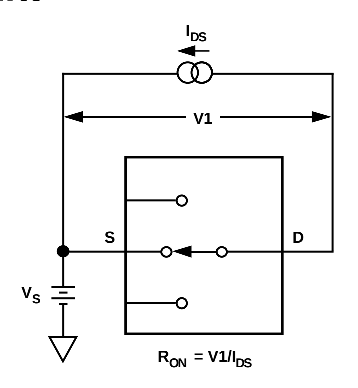
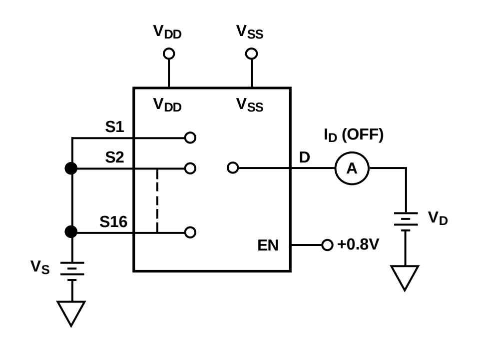


Figure 16. Crosstalk vs. Frequency

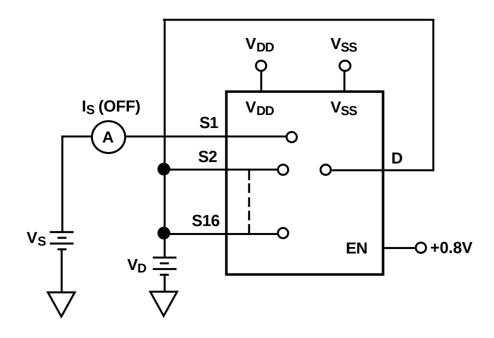
Test Circuits



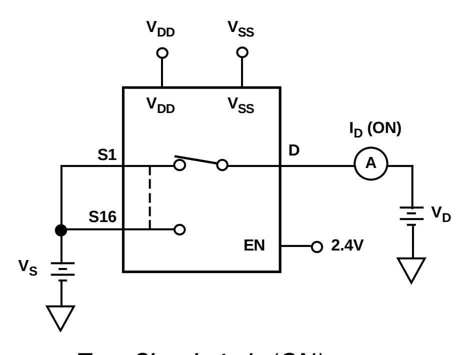
Test Circuit 1. On Resistance



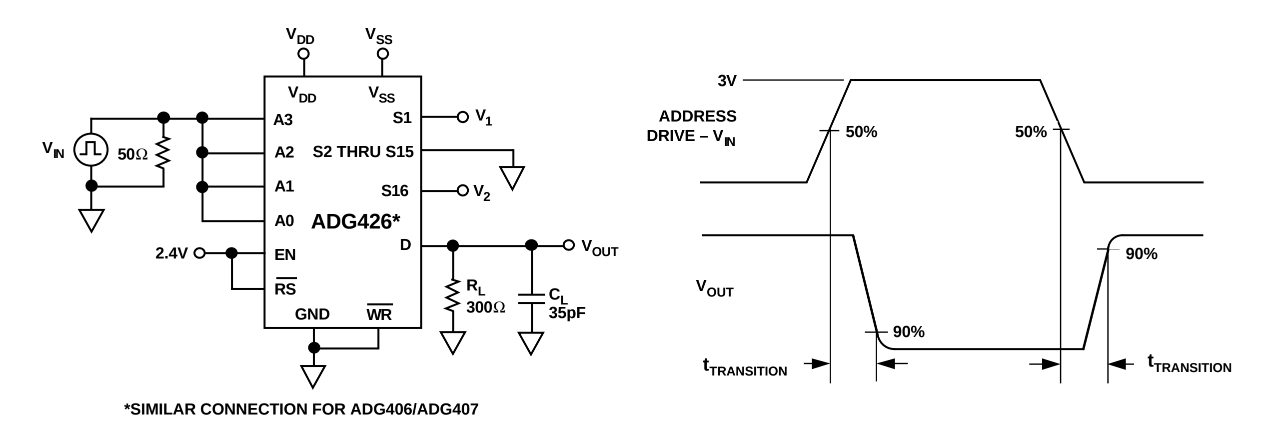
Test Circuit 3. I_D (OFF)



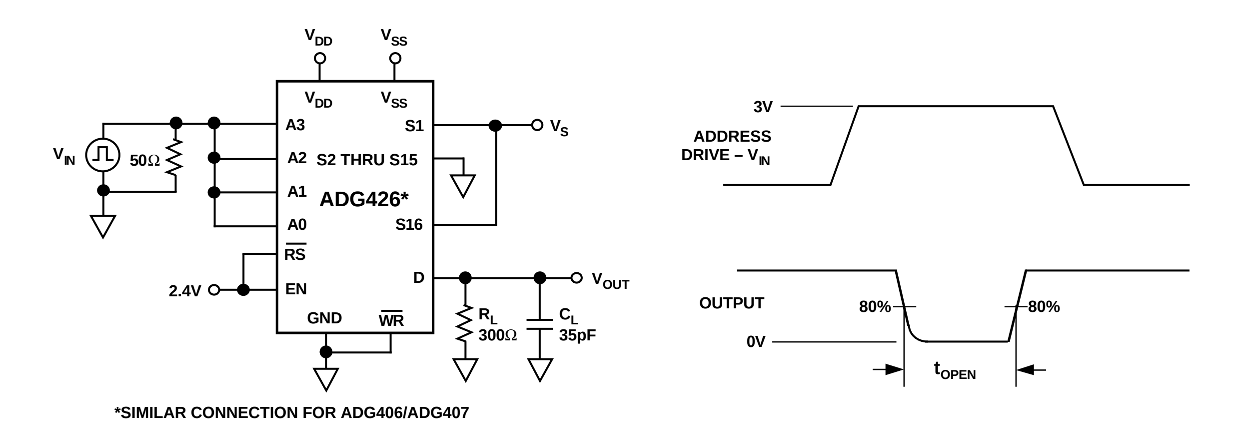
Test Circuit 2. I_S (OFF)



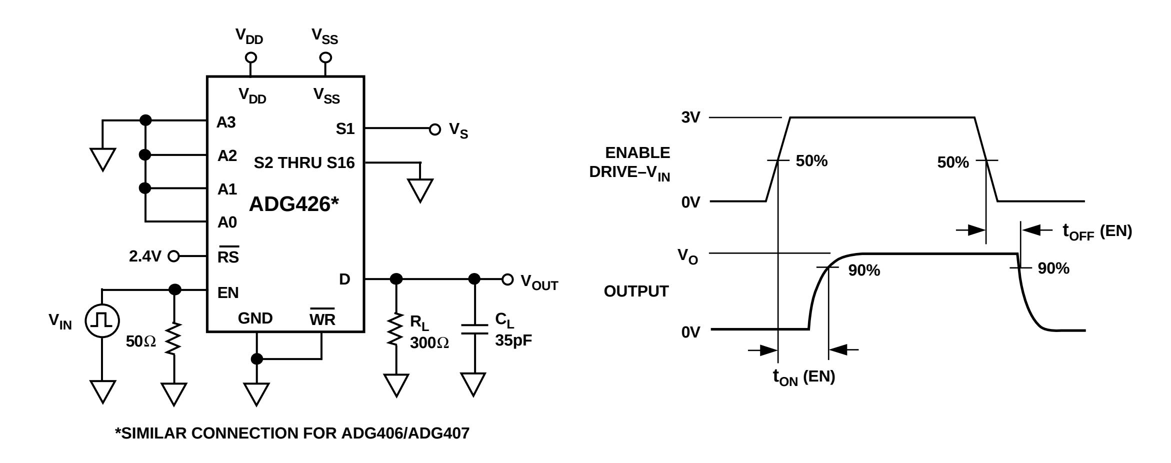
Test Circuit 4. I_D (ON)



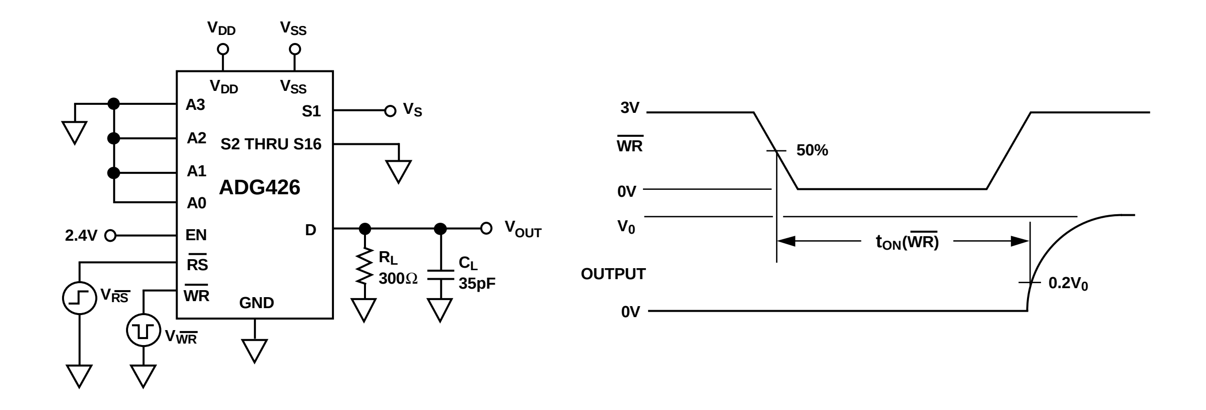
Test Circuit 5. Switching Time of Multiplexer, $t_{TRANSITION}$



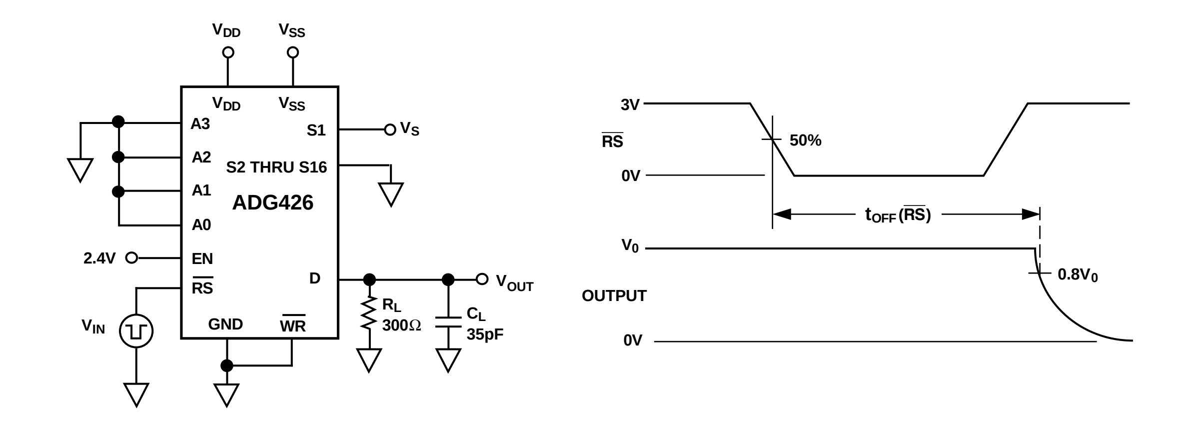
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}



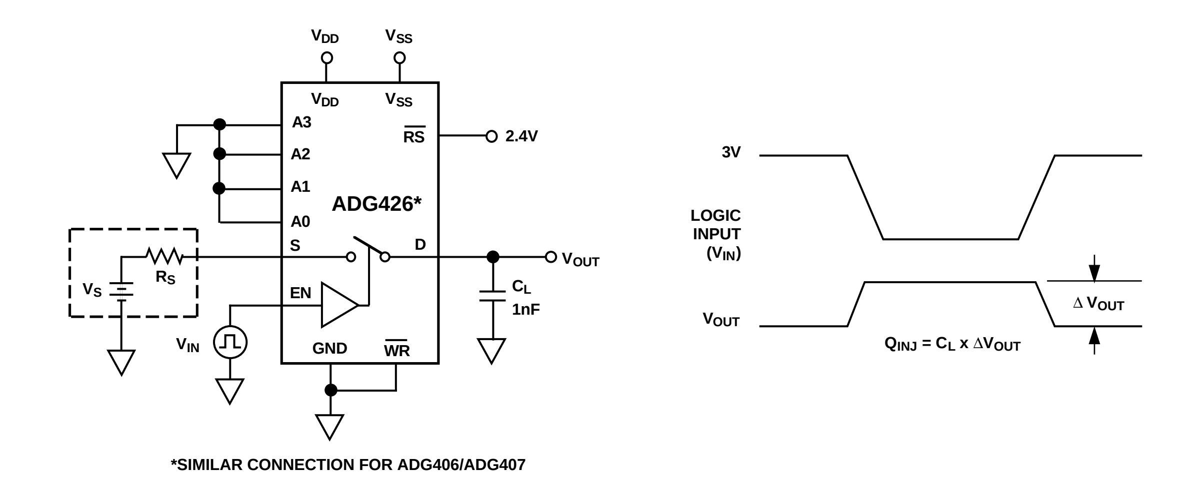
Test Circuit 7. Enable Delay, t_{ON} (EN), t_{OFF} (EN)



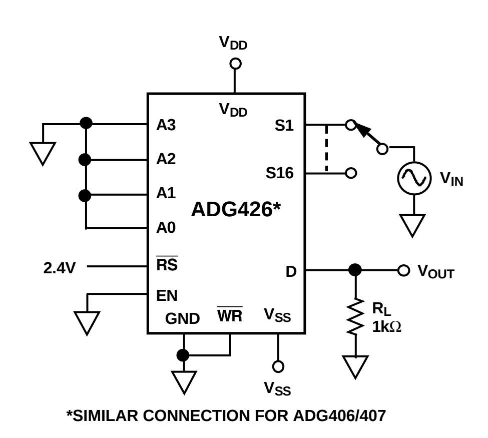
Test Circuit 8. Write Turn-On Time, t_{ON} ($\overline{WR}$)



Test Circuit 9. Reset Turn-Off Time, t_{OFF} ($\overline{RS}$)



Test Circuit 10. Charge Injection



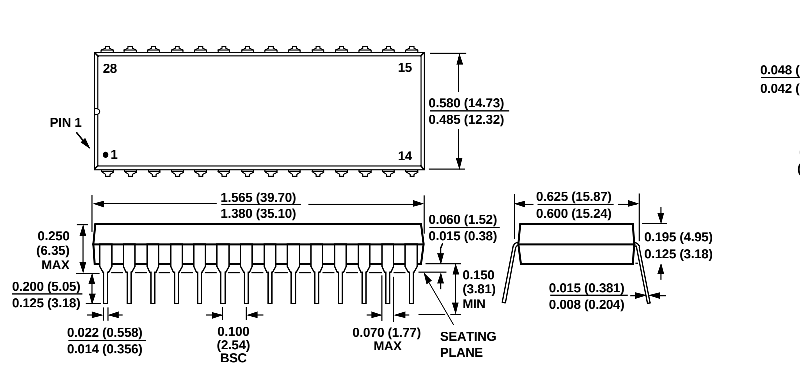
Test Circuit 11. OFF Isolation

Test Circuit 12. Crosstalk

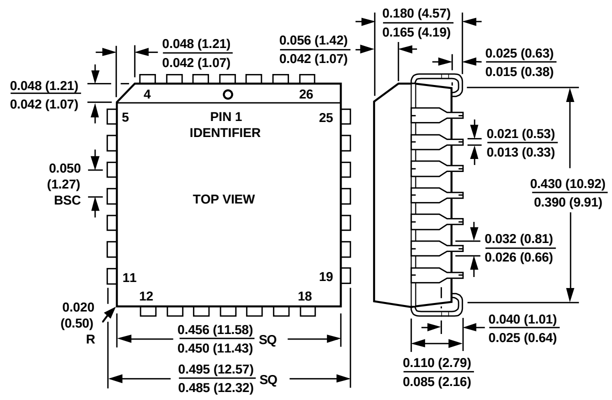
OUTLINE DIMENSIONS

Dimensions shown in inches an (mm).

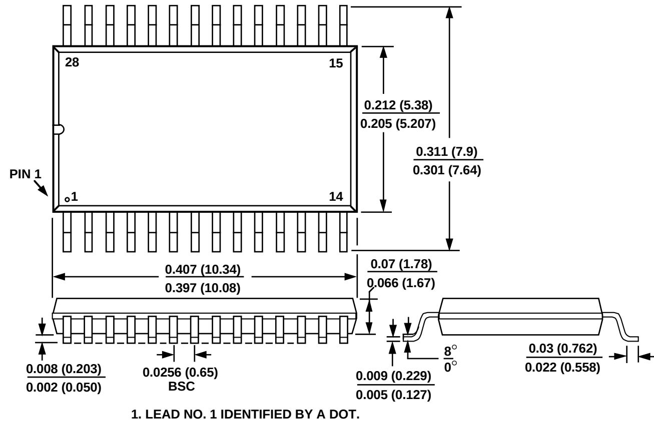
28-Pin Plastic (N-28)



28-Pin PLCC (P-28A)



28-Pin SSOP (RS-28)



1. LEAD NO. 1 IDENTIFIED BY A DOT.
2. LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS

C1905–18–4/94

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